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L2: Entry 21 of 52 File: USPT May 27, 1997

DOCUMENT-IDENTIFIER: US 5634076 A
TITLE: DMA controller responsive to transition of a request signal between first state and second state and maintaining of second state for controlling data transfer

ABPL:
A monolithic digital signal processor includes a core processor for performing digital signal computations, an I/O processor for controlling external access to and from the digital signal processor through an external port, first and second memory banks for storing instructions and data for the digital signal computations, and first and second buses interconnecting the core processor, the I/O processor and the memory banks. The core processor and the I/O processor access the memory banks on the first bus without interference on different clock phases of a clock cycle. The internal memory and the I/O processor of the digital signal processor are assigned to a region of a global memory space, which facilitates multiprocessing configurations. In a multiprocessor system, each digital signal processor is assigned a processor ID. The digital signal processor includes a bus arbitration circuit for controlling access to an external bus through the external port. The digital signal processor may include one or more serial ports and one or more link ports for point-to-point communication with external devices. A DMA controller controls DMA transfers through the external port, the serial ports and the link ports.

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L2: Entry 23 of 52 File: USPT Mar 11, 1997

DOCUMENT-IDENTIFIER: US 5611075 A
TITLE: Bus architecture for digital signal processor allowing time multiplexed access to memory banks

ABPL:
A monolithic digital signal processor includes a core processor for performing digital signal computations, an I/O processor for controlling external access to and from the digital signal processor through an external port, first and second memory banks for storing instructions and data for the digital signal computations, and first and second buses interconnecting the core processor, the I/O processor and the memory banks. The core processor and the I/O processor access the memory banks on the first bus without interference on different clock phases of a clock cycle. The internal memory and the I/O processor of the digital signal processor are assigned to a region of a global memory space, which facilitates multiprocessing configurations. In a multiprocessor system, each digital signal processor is assigned a processor ID. The digital signal processor includes a bus arbitration circuit for controlling access to an external bus through the external port. The digital signal processor may include one or more serial ports and one or more link ports for point-to-point communication with external devices. A DMA controller controls DMA transfers through the external port, the serial ports and the link ports.

L2: Entry 41 of 52 File: JPAB Jun 21, 1980

DOCUMENT-IDENTIFIER: JP 55082366 A
TITLE: MULTIPROCESSOR SYSTEM

FPAR:
PURPOSE: To make it possible to access a shared memory unit without any mutual influence of processors by providing two processors using non-duplicate two-phase clocks and the shared memory unit shared by them.

FPAR:
CONSTITUTION: Clocks ϕ1 and ϕ2 of master-side microprocessor 2 are shifted in phase from clocks ϕ1 and ϕ2 of slave-side microprocessor 3 by 180° respectively. DMAC control signal G is high-level for high-level clock ϕ2 of processor 2 and is fixed-level for low-level clock ϕ2 of processor 2. That is, processor 2 is connected to shared memory unit 7 when clock ϕ2 of the master-side microprocessor is high-level, and processor 3 is connected to shared memory unit 7 when clock ϕ2 of the slave- side microprocessor is high-level. In case of read access of processors 2 and 3, they are not affected by each other because busses between them and shared memory unit 7 are disconnected.

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L2: Entry 52 of 52 File: DWPI May 27, 1981

DERWENT-ACC-NO: 1981-F1899D
DERWENT-WEEK: 198123

TITLE: Multi-processor system resource allocation control - identifies available resource and requesting processor during complementary-phase clock cycles

ABTX:
The processors alternately address the memory during one phase of the clock and read or write data in the memory during the other phase. An indicator of availability of the shared memory is scanned and after a waiting cycle its utilisation is authorised if available to the requesting processor..

ABEQ:
The processors alternately address the memory during one phase of the clock and read or write data in the memory during the other phase. An indicator of availability of the shared memory is scanned and after a waiting cycle its utilisation is authorised if available to the requesting processor..